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Chantilly, VA 20151

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Intel Legal Team

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Page 1 of 54

Urgent

Confidential

Date: October 28, 2004

To:	**Fax:**	**Art Unit:**
Examiner:	**(703) 872-9306**	2826
Alexander O. Williams		
USPTO		
From:	**Fax:**	**M/S:**
Jay P. Beale	703-633-3303	

Subject: A Process of Vertically Stacking Multiple Wafers Supporting Different...
Application No.: 10/066,643; Inventor: Kellar et. al.
Filed: 2/6/2002 Docket No. 042390.P12752

A CONFIRMATION COPY OF THIS DOCUMENT:

WILL NOT BE SENT

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Serita Evans **Date: 10/28/04** Serita Evans

Included in this transmission:
Fax Cover Sheet (1 page)
RCE Transmittal - PTO/SB30 (1 page submitted in duplicate)
Preliminary Amendment (3 pages)
Figures 1A-B, 2-5 and 6A-B (4 pages)
Information Disclosure Statement w/ PTO-1449 (5 pages)
One non-US reference (15 pages)
One non-published application (24 pages)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/066,643	Confirmation No.: 4503
Applicant	:	Kellar, et al.	
Filed	:	February 6, 2002	
TC/AU	:	2826	
Examiner	:	Williams, Alexander O.	
Docket No.	:	42390.P12752	
Customer No.	:	08791	

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Preliminary Amendment

Examiner,

This Preliminary Amendment accompanies the filing of a Request for Continuing Examination in this application.

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.

CERTIFICATE OF TRANSMISSION

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By: Serita Evans

Date: October 28, 2004

Amendments to the Specification

Please insert the following paragraph before the first paragraph in the specification:

This application is related to the following patents and pending patent applications, which are assigned to the assignee of this application: US Patent 6,661,085, filed on February 6, 2002 and issued on December 9, 2003; US Patent Application serial number 10/066,645, filed on February 6, 2002; US Patent 6,762,076, filed on February 20, 2002 and issued on July 13, 2004; US Patent Application serial number 10/613,006, filed on July 7, 2003; US Patent Application serial number 10/695,328, filed on October 27, 2003; and US Patent Application serial number 10/855,032, filed on May 26, 2004.

219.40232X00
LID#: P12070

CLAIMS:

1. A method of vertically stacking wafers, comprising:

selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers;

bonding the adjacent wafers, via respective metallic lines on opposing surfaces of the adjacent wafers, to establish electrical connections between active devices on vertically stacked wafers; and

forming one or more vias to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect.

2. The method as claimed in claim 1, wherein each via is formed by:

selectively etching the top wafer to form a via;

depositing an oxide layer to insulate a sidewall of the via;

forming a barrier/seed layer in the via; and

depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection between active devices on the vertically stacked wafers and the external interconnect.

3. The method as claimed in claim 1, wherein the metallic lines are Copper (Cu) lines deposited to serve as electrical contacts between active devices on the vertically stacked wafers.

4. The method as claimed in claim 2, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy.

5. The method as claimed in claim 2, wherein the barrier/seed layer contains a barrier layer deposited in the via, and a copper (Cu) seed layer deposited in the trench overlying the barrier layer.

6. The method as claimed in claim 5, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

7. The method as claimed in claim 1, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

8. The method as claimed in claim 1, wherein the vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

9. The method as claimed in claim 1, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of a via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

selectively etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and an external interconnect.

10. The method as claimed in claim 9, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier

layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

11. The method as claimed in claim 1, wherein the vias are formed during a Shallow Trench Isolation (STI) process in the top wafer before the adjacent wafers are bonded, via the respective metallic lines deposited on opposing surfaces of the adjacent wafers.

12. A method of forming vertically stacked wafers, comprising:

depositing a plurality of metallic lines on opposing surfaces of top and bottom wafers;

forming a conductive plug;

bonding the adjacent wafers, via respective metallic lines, to form vertically stacked wafers; and

forming at least one via on the top wafer to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect, by selectively etching through the top wafer until stopped by the conductive plug, depositing an oxide layer to insulate a sidewall of the via, depositing a barrier/seed layer on the bottom of the via, and filling the via with a conduction metal to serve as electrical connections between active devices on the vertically stacked wafers and the external interconnect.

13. The method as claimed in claim 12, wherein the metallic lines are Copper (Cu) lines deposited to serve as electrical contacts between active devices on the vertically stacked wafers.

14. The method as claimed in claim 12, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy.

15. The method as claimed in claim 12, wherein the barrier/seed layer contains a barrier layer deposited in the via, and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

16. The method as claimed in claim 15, wherein the barrier layer is comprised of a material selected from one of the group including tantalum, titanium, and tungsten, and the Cu seed layer is comprised of a few layers of copper (Cu) atoms deposited on the barrier layer by chemical vapor deposition (CVD) process.

17. The method as claimed in claim 12, further comprising dummy vias arranged on opposing surfaces of the adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active devices on the vertically stacked wafers.

18. The method as claimed in claim 12, wherein the via is formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the adjacent wafers.

19. A three-dimensional (3-D) vertically stacked wafer system, comprising:

a first wafer including an active region to support one or more integrated circuit (IC) devices;

a second wafer including an active region to support one or more integrated circuit (IC) devices;

metallic lines deposited on opposing surfaces of the first and second wafers at designated areas to establish metal bonding between the first and second wafers in a stack and provide electrical connections between active IC devices on the first and second wafers in the stack; and

one or more vias formed, via the active region of the first wafer, to serve as electrical connections between the active IC devices on the first and second wafers in the stack and an external interconnect.

20. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 19, wherein the metallic lines include Copper (Cu) lines deposited on opposing surfaces of the first and second wafers to serve as electrical contacts between active IC devices on the first and second wafers.

21. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each via is formed by:

selectively etching the first wafer to form a via;

depositing an oxide layer to insulate a sidewall of the via;

forming a barrier/seed layer in the via; and

depositing a conduction metal on the barrier/seed layer in the via for providing an electrical connection between active IC devices on the vertically stacked wafers and the external interconnect.

22. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 21, wherein the conduction metal deposited in the via is copper (Cu) or a Cu alloy, and the barrier/seed layer includes a barrier layer deposited in the via overlying the oxide layer and a copper (Cu) seed layer deposited in the via overlying the barrier layer.

23. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 22, wherein the barrier layer is comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and the Cu seed layer is comprised of a thin layer of copper (Cu) deposited on the barrier layer by chemical vapor deposition (CVD) process.

24. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of the via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

etching the oxide layer in the upper trench section to form a lower trench section of the via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active devices on the vertically stacked wafers and the external interconnect.

25. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 24, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum nitride (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

26. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 20, wherein the vias are formed during a Shallow Trench Isolation (STI) process in the first wafer before the first and second wafers are bonded, via the respective metallic lines deposited on opposing surfaces of the first and second wafers.

27. A three-dimensional (3-D) vertically stacked wafer system, comprising:

a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and provide electrical connections between active IC devices on the adjacent wafers;

a first stack of wafers in which adjacent wafers are bonded, via metallic lines deposited on opposing surfaces of the adjacent wafers at designated areas to establish metal bonding between the adjacent wafers and provide electrical connections between active IC devices on the adjacent wafers; and

one or more vias formed on opposing surfaces of the first stack of wafers and the second stack of adjacent wafers to serve as electrical connections between the active IC devices on the first and second stacks of wafers and an external interconnect.

28. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the metallic lines include Copper (Cu) lines deposited on opposing surfaces of the adjacent wafers in the first and second stacks of wafers to serve as electrical contacts between active IC devices on the first and second stacks of wafers.

29. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, further comprising dummy vias arranged on opposing surfaces of the first and second stacks of adjacent wafers to increase the surface area for wafer-to-wafer bonding and serve as auxiliary structures such as ground planes or heat conduits for the active IC devices on vertically stacked wafers.

30. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein the vias are formed tapered from the top to the bottom via trench to increase the surface area for wafer to-wafer bonding in the first and second stacks of adjacent wafers.

31. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 27, wherein each via is formed by a dual damascene process comprised of:

selectively etching the top wafer to form an upper trench section of a via;

depositing an oxide layer to insulate a sidewall of the upper trench section of the via;

etching the oxide layer in the upper trench section of the via to form a lower trench section of the via;

depositing a barrier/seed layer in the upper trench section and the lower trench section of the via; and

depositing a conduction metal on the barrier/seed layer for providing an electrical connection between active IC devices on the vertically stacked wafers and the external interconnect.

32. The three-dimensional (3-D) vertically stacked wafer system as claimed in claim 31, wherein the barrier/seed layer includes a barrier layer comprised of a material selected from one of the group including tantalum (Ta), tantalum (TaN), titanium (Ti), and tungsten (W), and deposited in the upper trench section overlying the oxide layer and the lower trench section of the via; and a copper (Cu) seed layer comprised of a thin layer of copper (Cu) deposited on the barrier layer, and deposited overlying the barrier layer in both the upper trench section and the lower trench section of the via.

ABSTRACT OF DISCLOSURE

A method of vertically stacking wafers is provided to form three-dimensional (3D) wafer stack. Such method comprising: selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers; bonding the adjacent wafers, via the metallic lines, to establish electrical connections between active devices on vertically stacked wafers; and forming one or more vias to establish electrical connections between the active devices on the vertically stacked wafers and an external interconnect. Metal bonding areas on opposing surfaces of the adjacent wafers can be increased by using one or more dummy vias, tapered vias, or incorporating an existing copper (Cu) dual damascene process.

Remarks

Applicants respectfully request entry of the amendments to the specification offered herein. Applicants have also taken this opportunity to present formal drawings **(Figs. 1A-B, 2-5 and 6A-B)**. If the Examiner has any questions, Examiner is invited to contact the undersigned at (703) 633-0927. If any fee insufficiency or overpayment is found, please charge the insufficiency or credit the overpayment to Deposit Account 50-0221.

Respectfully submitted,

Dated: 28 Oct 04

Jay Beale,
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Reg. No. 50,901

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Chantilly, VA 20151
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PTO/SB/30 (09-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/066,643
Filing Date	February 6, 2002
First Named Inventor	Scot A. Kellar
Art Unit	2826
Examiner Name	Alexander O. Williams
Attorney Docket Number	042390.P12752

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This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☑ Information Disclosure Statement (IDS)

      iv. ☑ Other Formal Dwgs: Figs. 1A-B, 2-5 and 6A-B

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0221

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Jay Beale	Registration No. (Attorney/Agent)	50,901
Signature		Date	28 Oct. '04

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Name (Print/Type)	Serita Evans		
Signature		Date	10/28/04

PTO/SB/30 (09-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

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P.O. Box 1450
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Application Number	10/066,643
Filing Date	February 6, 2002
First Named Inventor	Scot A. Kellar
Art Unit	2826
Examiner Name	Alexander O. Williams
Attorney Docket Number	042390.P12752

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      i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☑ Information Disclosure Statement (IDS)

      iv. ☑ Other Formal Dwgs: Figs. 1A-B, 2-5 and 6A-B

2. Miscellaneous

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED			
Name (Print/Type)	Jay Beard	*Registration No. (Attorney/Agent)*	50,901
Signature		*Date*	28 Oct. '04

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Name (Print/Type)	Serita Evans		
Signature		*Date*	10/28/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/066,643	Confirmation No.: 4503
Applicant	:	Kellar, et al.	
Filed	:	February 6, 2002	
TC/AU	:	2826	
Examiner	:	Williams, Alexander O.	
Docket No.	:	42390.P12752	
Customer No.	:	08791	

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement under 37 C.F.R. 1.97

Examiner,

Please consider the documents cited in the accompanying Information Disclosure Statement form during the examination of the above-referenced patent application. It is respectfully requested that the IDS form be initialed by the Examiner to indicate such consideration, and that a copy of the initialed form be returned to the applicants. This IDS is being submitted before the mailing of a first action on the merits.

The documents listed in the IDS are cited in the following related patents and pending patent applications, which are assigned to the assignee of the present application: US Patent 6,661,085, filed on February 6, 2002 and issued on December 9, 2003; US Patent Application serial number 10/066,645, filed on February 6, 2002; US Patent 6,762,076, filed on February 20, 2002 and issued on July 13, 2004; US Patent Application serial number 10/613,006, filed on July 7, 2003; US Patent Application serial number 10/695,328, filed on October 27, 2003; and US Patent Application serial number 10/855,032, filed on May 26, 2004.

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Respectfully submitted,

Dated: 28Oct, '04

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By: _____
Sonia Evans

Date: October 28, 2004

PTO/SB/08a (08-03)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete If Known	
Application Number	10/066,643
Filing Date	February 6, 2002
First Named Inventor	Kellar
Art Unit	2828
Examiner Name	Williams, Alexander O.
Attorney Docket Number	42390.P12752

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 4,689,113		8/25/1987	Balasubramanyam, et	
		US- 6,559,042		5/6/2003	Barth, et al.	
		US- 5,241,450		8/31/1993	Bernhardt, et al.	
		US- 5,880,010		3/9/1999	Davidson	
		US- 5,656,554		8/12/1997	Desai, et al.	
		US- 6,468,098		10/22/2002	Eldridge	
		US- 6,355,976		3/12/2002	Faris	
		US- 6,594,025		7/15/2003	Forouhi	
		US- 6,355,501		3/12/2002	Fung, et al.	
		US- 20020163072	A1	11/7/2002	Gupta, et al.	
		US- 5,627,106		5/6/1997	Hsu	
		US- 5,419,806		5/30/1995	Huebner	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		EP0293459B1	7/22/1992	Carlomagno		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/066,643
Filing Date	February 6, 2002
First Named Inventor	Keitar
Art Unit	2826
Examiner Name	Williams, Alexander O.
Attorney Docket Number	42390.P12752

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,473,197		12/5/1995	Idaka, et al.	
		US- 6,661,085		12/9/2003	Kellar, et al.	
		US- 20040142540	A1	7/22/2004	Kellar, et al.	
		US- 20030157782	A1	7/21/2003	Kellar, et al.	
		US- 20040014308	A1	1/22/2004	Kellar, et al.	
		US- 6,762,076		7/13/2004	Kim, et al.	
		US- 10/855,032			Kim, et al.	
		US- 5,455,445		10/3/1995	Kurtz, et al.	
		US-6,504,263		1/7/2003	Mastromatteo, et al.	
		US- 5,998,808		12/7/1999	Matsushita	
		US- 6,255,726		7/3/2001	Vindasius, et al.	
		US- 5,366,906		11/22/1994	Wojnarowski, et al.	
		US- 6,100,181		8/8/2000	You, et al.	
		US- 5,773,988		6/30/1998	Thompson, et al.	
		US- 20030079836	A1	5/1/2003	Lin, et al.	
		US- 6,724,084		4/20/2004	Hikita, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]–Number[4]–Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 3 of 3

Complete if Known	
Application Number	10/068,643
Filing Date	February 6, 2002
First Named Inventor	Kellar
Art Unit	2826
Examiner Name	Williams, Alexander O.
Attorney Docket Number	42390.P12752

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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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